WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a substrate at least having an insulative surface;

a semiconductor film provided on said surface of said substrate comprising a first semiconductor layer of a first conductivity type, a second semiconductor layer of said first conductivity type having an impurity concentration lower than that of said first semiconductor layer, a third semiconductor layer of a second conductivity type opposite to said first conductivity type and a fourth semiconductor layer of said second conductivity type having an impurity concentration lower than that of said third semiconductor layer; and

an insulative isolator formed on a surface of said semiconductor film on the far side from said substrate, separately from said surface of said substrate, wherein

said second and fourth semiconductor layers form a pn junction extending in the thickness direction of said semiconductor film, and

a maximum value of a distance between said pn junction and a boundary between said isolator and said semiconductor film is not more than 2μm, when a direction from said boundary to said isolator along said surface of said substrate is taken as a positive direction.

2. The semiconductor device according to claim 1, wherein

said pn junction has a portion separated from said isolator.

3. The semiconductor device according to claim 2, wherein

said portion of said pn junction separated from said isolator forms a semiconductor element.

4. The semiconductor device according to claim 3, wherein

said first, second, fourth and third semiconductor layers are adjacent to each other in this order, and

said first and third semiconductor layers function as a contact with respect to said pn junction.

5. The semiconductor device according to claim 2, wherein

said first, fourth, second and third semiconductor layers are adjacent to each other in this order, and

said first and second semiconductor layers function as source/drain layers of MOS transistors having conductivity types different from each other, respectively.

6. The semiconductor device according to claim 2, further comprising

a cover having an insulative surface in contact with said portion of said pn junction separated from said isolator.

7. The semiconductor device according to claim 5, further comprising

a cover having an insulative surface in contact with said portion of said pn junction separated from said isolator.

8. The semiconductor device according to claim 2, wherein

said second semiconductor layer is provided in said fourth semiconductor layer,

said first semiconductor layer includes a pair of first semiconductor layers being formed in said second semiconductor layer, and

said pair of first semiconductor layers function as a contact with respect to said second semiconductor layer.

9. A semiconductor device comprising:

a substrate at least having an insulative surface;

a semiconductor film provided on said surface of said substrate, having at least one pn junction extending in a thickness direction of said substrate, said at least one pn junction including a pn junction which is applied with voltage; and

a metallic compound layer selectively formed on said semiconductor film, being a compound of said semiconductor film and metal, wherein

a maximum value of a distance between at least said pn junction which is applied with voltage and a boundary between said metallic compound layer and said semiconductor film is not more than 2μm, when a direction from said boundary to said semiconductor film along said surface of said substrate is taken as a positive direction.

10. The semiconductor device according to claim 9, further comprising

a mask provided on said at least one pn junction for preventing silicidation with metal of said semiconductor film.

11. The semiconductor device according to claim 11, wherein

said mask has the same structure as a gate of a MOS transistor to be formed on said semiconductor film in a thickness direction thereof.

12. A resistor comprising:

a substrate at least having an insulative surface;

a first semiconductor layer of a first conductivity type provided on said surface of said substrate;

an insulative isolator formed on a surface of said first semiconductor film on the far side from said substrate, separately from said surface of said substrate; and

a second semiconductor layer of a second conductivity type opposite to said first conductivity type formed in said first semiconductor layer, said second semiconductor layer forming a pn junction in conjunction with said first semiconductor layer, said pn junction extending from said surface of said first semiconductor layer to said surface of said substrate and being separated from said isolator.

13. The resistor according to claim 12, further comprising

a pair of third semiconductor layers of said second conductivity type formed in said second semiconductor layer, having an impurity concentration higher than that of said second semiconductor layer.

14. The resistor according to claim 13, further comprising

a gate electrode covering said pn junction.

15. The resistor according to claim 13, further comprising

a cover having an insulative surface in contact with said portion of said pn junction separated from said isolator.